AMENDMENTS TO THE CLAIMS

1. (Currently Amended) An apparatus, comprising:

a buffer having ~~at least one~~ a trigger, integrated on a component connected with a simultaneous bi-directional (SBD) memory bus having ternary logic levels, to facilitate ~~observe~~ observing and ~~echo~~ echoing of one or more of a ~~predetermined finite set of bi-direction~~ plurality of signals transmitted on said memory bus, wherein the trigger operates to instruct the buffer using one or more of the following: a control signal-based indication, an address signal-based indication, and a time-based indication.

2. (Original) The apparatus as in claim 1, further comprising an observability port coupled with said buffer to receive said echoed signals, an observability bus connected with said observability port, and a diagnostic device being at least one of a logic analyzer and a bus analyzer connected with said observability bus and performing at least one of detecting said echoed signals, accessing said echoed signals and reading said echoed signals.

3. (Original) The apparatus as in claim 2, wherein said observability port is a logic observability port.

Claims 4-5 (Cancelled)

6. (Currently Amended) A method, comprising:

transmitting a plurality of signals on a simultaneous bi-directional (SBD) memory bus having ternary logic levels;

a buffer having ~~at least one~~ a trigger, integrated on a component connected with the bus, to facilitate observing and echoing of one or more of a ~~predetermined finite set of~~ plurality of signals transmitted on the bus,

wherein the trigger operates to instruct the buffer using one or more of the following: a control signal-based indication, an address signal-based indication, and a time-based indication.

7. (Original) The method as in claim 6, further comprising:

receiving said echoed signals; and

performing at least one of detecting said echoed signals, accessing said echoed signals and reading said echoed signals.

Claims 8-13 (Cancelled)

14. (Currently Amended) A system, comprising:

a memory;

an input/output (I/O) port; ~~and~~

a microprocessor; and

a buffer, having ~~at least one~~ a trigger, integrated on a component coupled with a simultaneous bi-directional (SBD) memory bus having ternary logic levels, to facilitate ~~observe and echo a predetermined finite set of bi-direction~~ observing and echoing of a plurality of signals transmitted on said bus, wherein the trigger operates to instruct the buffer using one or more of the following: a control signal-based indication, an address signal-based indication, and a time-based indication.

15. (Original) The system as in claim 14, further comprising an observability port coupled with said buffer to receive said echoed signals, an observability bus connected with said observability port, and a diagnostic device being at least one of a logic analyzer and a bus analyzer connected with said observability bus and

performing at least one of detecting said echoed signals, accessing said echoed signals and reading said echoed signals.

16. (Original) The system as in claim 15, wherein said observability port is a logic observability port.

Claims 17-18 (Cancelled)